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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/686,304	10/11/2000	Paul W. Dent	8194-416/P11717-US1	5164

20792 7590 03/08/2004

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	4

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/686,304	DENT, PAUL W.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-47, 67-96 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakoda et al U.S. patent No 6,519,292 B1.

As per claims 1, 16, 45, 67 and 90 Sakoda teaches a communications system for communicating with a plurality of terminals, the system comprising: a network station; a variable error correction encoder that error correction encodes (see figs. 6, 14 and 16 element 43 and col.1, lines 63-65 and col.9,lines 32-40) respective bit streams for respective ones of the plurality of terminals according to respective selected coding rates of a plurality of coding rates; a variable symbol generator that maps (see element 48 and col.10, lines 1-5) respective ones of the error correction coded bit streams to respective symbol streams according to respective signal constellations of a plurality of signal constellations of various orders; a variable spreader (see

block of elements 44-47 and col.9, lines 38-67) that spreads the respective symbol streams according to respective orthogonal spreading codes of a plurality of mutually orthogonal spreading codes of various lengths; a transmitter that transmits (see element 49 and col.10, lines 6-14) the spread symbol streams from the network station in a communications medium; and a controller (see element 42 and col.10, lines 15-67 and col.11, lines 30-67 and col.18, lines 33-38), operatively associated with the variable error correction encoder, the variable symbol generator and the variable spreader, that selects respective combinations of coding rate, signal constellation and spreading code applied to the respective bit streams such that the spread symbol streams transmitted from the network station are spread according to mutually orthogonal spreading codes.

As per claim 2, Sakoda does include wherein the controller (see element 42 and col.10, lines 15-67 and col.11, lines 30-67) selects the respective combinations of coding rate, signal constellation and spreading codes applied to the respective bit streams such that each of the bit streams is transmitted at an information transmission rate that is greater than or equal to a predetermined information transmission rate and with a signal transmission quality that meets a predetermined criterion.

As per claims 3-6 Sakoda does include, wherein the controller selects the respective combinations of coding rate (see col.9, lines 42-46 and col.18, lines 49-55), signal constellation and spreading code applied to the respective bit streams to maximize an information transmission rate for a selected terminal of the plurality of terminals.

As per claim 7, Sakoda inherently includes wherein the selected terminal comprises a web browser.

As per claim 8, Sakoda inherently includes wherein the variable error correction encoder comprises at least one of a convolutional encoder, a Trellis encoder, a serial concatenation of two encoders connected by an interleaver and a turbo encoder.

As per claim 9, Sakoda inherently includes wherein the plurality of signal constellations comprises at least one of a QPSK constellation, an offset QPSK constellation, an MPSK constellation, and an M-QAM constellation, wherein M is greater than or equal to eight.

As per claim 10, Sakoda does include wherein the plurality of orthogonal spreading codes comprises a plurality of Walsh-Hadamard codes.

As per claim 11, Sakoda does include, wherein the variable spreader spreads the respective symbol streams according to respective combinations of an orthogonal spreading code of the plurality of orthogonal spreading code and a common scrambling (see col.9, lines 48-55) code that is applied to each of the symbol streams.

As per claim 12, Sakoda inherently includes wherein the plurality of orthogonal spreading codes comprises a plurality of Walsh-Hadamard codes.

As per claim 13, Sakoda inherently includes wherein the common scrambling code comprises a sequence of QPSK symbols.

As per claim 14, Sakoda does include, wherein respective ones of the combinations of orthogonal spreading code and the common scrambling code (see figs. 6, 14 and 16 and col.9, lines 48-55) are respective multiplicative combinations, and wherein the variable spreader complex multiplies respective ones of the symbol streams by the respective multiplicative combinations such that one of four phase changes in steps of ninety degrees is provided for each symbol repeat produced.

As per claim 15, Sakoda does include wherein the variable spreader spreads respective ones of the symbol streams according to respective combinations of a Fourier (see fig.14, element 107) code and a common scrambling code that is applied to each of the symbol streams, wherein the Fourier codes applied to the symbol streams are mutually orthogonal.

As per claim 17, Sakoda inherently includes wherein the plurality of selectable signal constellations includes at least two signal constellations of different order.

As per claim 18, Sakoda does include further comprising a controller (see element 42), operatively associated with the variable symbol generator that selects the signal constellation to provide a desired information transmission rate for the bit stream.

As per claim 19, Sakoda inherently includes, wherein the controller selects the signal constellation used by the variable symbol generator based on signal transmission quality.

As per claim 20, Sakoda inherently includes, wherein the error correction encoder comprises a variable error correction encoder that encodes the bit stream according to a selected error correction code of a plurality of selectable error correction codes.

As per claim 21, Sakoda does include comprising a controller (see element 42), operatively associated with the variable error correction encoder and the variable symbol generator and the variable spreader, that selects the error correction code used by the variable error correction encoder and the signal constellation used by the variable symbol generator to provide a desired information transmission rate for the bit stream.

As per claim 22, Sakoda inherently includes wherein the controller selects the error correction code used by the error correction encoder and the signal constellation used by the variable symbol generator based on signal transmission quality.

As per claim 23, Sakoda inherently includes: wherein the error correction encoder comprises a variable error correction encoder that encodes the bit stream according to a selected error correction code of a plurality of selectable error correction codes; and wherein the spreader comprises a variable spreader that spreads the symbol according to a selected spreading code of a plurality of selectable orthogonal spreading codes including at least two spreading codes of different lengths.

As per claim 24, Sakoda inherently includes further comprising a controller, operatively associated with the variable error correction encoder, the variable symbol generator and the variable spreader, that selects the error correction code used by the variable error correction encoder, the signal constellation used by the variable symbol generator, and the spreading code used by the variable spreader to provide a desired information transmission rate for the bit stream.

As per claim 25, Sakoda inherently includes wherein the controller selects the error correction code used by the error correction encoder, the signal constellation used by the variable symbol generator, and the spreading code used by the variable spreader based on signal transmission quality.

As per claim 26, Sakoda inherently includes, wherein the controller selects the error correction encoding rate used by the variable error correction encoder, the signal constellation used by the variable symbol generator and the spreading code used by the variable spreader such that an information transmission rate for the bit stream is greater than a predetermined information transmission rate and a signal transmission quality for the bit stream meets a predetermined criterion.

As per claims 27, 31, Sakoda inherently includes: wherein the bit stream comprises a plurality of bit streams; wherein the variable error detection encoder error correction encodes respective ones of the plurality of bit streams according to respective selected error correction codes of the plurality of selectable error correction codes; wherein the variable symbol generator produces respective symbol streams from respective ones of the error correction encoded bit streams according to respective selected signal constellations of the plurality of selectable signal constellations; wherein the variable spreader spreads respective ones of the symbol streams according to respective selected spreading codes of the plurality of selectable spreading codes; and wherein the controller selects respective combinations of error correction code, signal constellation and spreading code applied to the respective bit streams of the plurality of bit streams such that an information transmission rate for a first bit stream exceeds a first minimum required information transmission rate associated with the first bit stream while an information transmission rate for a second bit stream is maintain at or above a second minimum required information transmission rate associated with the second bit stream.

As per claim 28, Sakoda inherently includes, wherein the controller selects respective combinations of error correction code, signal constellation and spreading code applied to the respective bit streams of the plurality of bit streams such that the information transmission rate for the first bit stream is maximized.

As per claim 29, Sakoda inherently includes, wherein the controller controls respective power levels at which respective ones of the plurality of bit streams are transmitted.

As per claim 30, Sakoda inherently includes, wherein the controller selects respective combinations of error correction code, signal constellation and spreading code applied to the

respective bit streams of the plurality of bit streams such that the information transmission rate for the first bit stream is maximized while maintaining a desired transmit power level for the plurality of bit streams.

As per claim 32, Sakoda inherently includes, wherein the set of orthogonal spreading codes comprises a set of Walsh-Hadamard codes.

As per claim 33, Sakoda includes, wherein the set of orthogonal spreading codes comprises a set of Fourier codes (see fig.14 element 107).

As per claim 34, Sakoda inherently includes, wherein the variable symbol generator produces respective symbols from the selected signal constellation from respective groups of bits of the encoded bit stream such that a first bit position of the successive groups of bits correlates to clusters of signal plane constellation points of the selected signal constellation and a second bit position of the successive groups correlates to relative positions within the clusters of constellation points.

As per claims 35, 36, Sakoda inherently includes further comprising means for determining respective first and second desired power levels for respective first and second recipients of information in respective ones of the first and second bit positions, and wherein the variable symbol generator controls spacing of the clusters of constellation points in the signal plane based on the determined first and second desired power levels.

As per claim 37, Sakoda includes, wherein the spreader comprises a multiplier (see element 44 or 46) that receives the symbol from the variable symbol generator and multiplies the received symbol by the spreading code to produce the spread symbol.

As per claim 38, Sakoda includes wherein the spreader further comprises a second multiplier that multiplies an orthogonal spreading code by a scrambling code to produce the spreading code (see figs.6, 14 and 16).

As per claim 39, Sakoda inherently includes wherein the spreader comprises: an orthogonal spreader that receives the symbol from the variable spreader and orthogonal spreads the received symbol according to a spreading code selected from a set of orthogonal spreading codes; and a scrambler that receives the orthogonal spread symbol and scrambles the orthogonal spread symbol according to a scrambling code to produce the spread symbol.

As per claim 40, Sakoda inherently includes: wherein the spreader comprises an orthogonal spreader that orthogonal spreads the error correction encoded bit stream according to a spreading code selected from a set of orthogonal spreading codes; wherein the variable symbol generator produces the symbol from the selected constellation from a group of bits of the orthogonal spread error correction encoded bit stream; and wherein the spreader further comprises a scrambler that receives the symbol produced by the variable symbol generator and scrambles the received symbol according to a scrambling code to produce the spread symbol.

As per claim 41, Sakoda inherently includes: wherein the spreader comprises an orthogonal spreader that orthogonal spreads the error -correction encoded bit stream according to a selected orthogonal spreading code of a set of orthogonal spreading codes; and wherein the plurality of selectable constellations includes at least one constellation that maps complementary bit patterns to diametrically opposite constellation points in a complex plane.

As per claim 42, Sakoda inherently includes wherein the spreader modulo-2 adds successive bits of the orthogonal spreading code to successive groups of bits of the error correction encoded bit stream.

As per claim 23, Sakoda inherently includes, wherein the variable error correction encoder comprises at least one of a convolutional encoder, a Trellis encoder, a turbo encoder, and a serial concatenation of a first error correction encoder, an interleaver and a second error correction encoder.

As per claim 44, Sakoda inherently includes, wherein the plurality of selectable signal constellations comprises at least one of a QPSK constellation, an 8PSK constellation, an M-ary PSK constellation, and a M-ary QAM constellation.

As per claim 46, Sakoda inherently includes further comprising means for determining respective first and second desired power levels for respective first and second recipients of information in respective ones of the first and second bit positions, and wherein the symbol generator controls spacing of the clusters of constellation points in the signal plane based on the determined first and second desired power levels.

As per claim 47, Sakoda inherently includes further comprising: means for determining respective first and second desired power levels for respective first and second recipients; and means for assigning respective ones of the first and second bit positions to respective ones of the first and second recipients based on the determined first and second desired power levels.

As per claim 48, Sakoda teaches receiving station, comprising: a receive (see fig. 15 element 120) r that receives a communications signal from a communications medium; a despreader (see block of elements 125-126) that despreads the received signal according to a

spreading code; a symbol estimator that generates a symbol estimate from the despread signal (see figs.8, 12, 15 elements s65, s94 s125 and col.3, lines 25-30 and col.5, lines 15-19 and col.12, lines 48-50); and a variable decoder (see figs. 8, 12, 15 elements 68, 95, 127) that decodes the symbol estimate according to a selected combination of an error correction code and a signal constellation of the plurality of selectable signal constellations.

As per claim 49, Sakoda inherently includes, wherein the plurality of selectable signal constellations comprises at least two signal constellations of different orders.

As per claim 50, Sakoda inherently includes wherein the variable decoder decodes the symbol estimate according to a selected error correction code of a plurality of error correction codes including at least two error correction codes of different rates.

As per claim 51, Sakoda inherently includes, wherein the despreader comprises a variable despreader that despreads the received signal according to a selected spreading code of a plurality of selectable spreading codes including at least two spreading codes of different lengths.

As per claim 52, Sakoda inherently includes, wherein the variable decoder comprises at least one of a Trellis decoder, a Viterbi decoder, and a turbo decoder.

As per claim 53, Sakoda inherently includes, wherein the symbol estimator comprises a RAKE combiner.

As per claim 54, Sakoda includes, wherein the despreader comprises a complex multiplier (see fig. 15 element 125).

As per claim 68, Sakoda inherently includes further comprising selecting a signal constellation for application to a bitstream of the plurality of bit streams to provide a desired information transmission rate for the bitstream.

As per claim 69, Sakoda inherently includes 7, further comprising selecting a signal constellation applied to a bitstream based on signal transmission quality.

As per claim 70, Sakoda inherently includes wherein the plurality of error correction codes includes at least two codes of different rates.

As per claim 71, Sakoda inherently includes, further comprising selecting the error Correction codes and signal constellation applied to a bitstream to provide a desired information transmission rate for the bitstream..

As per claim 72, Sakoda inherently includes, further comprising selecting the error correction code and the signal constellation applied to a bitstream based on signal transmission quality.

As per claim 73, Sakoda inherently includes, wherein the plurality of spreading codes comprises a plurality of spreading codes including at least two spreading codes of different lengths.

As per claim 74, Sakoda inherently includes, further comprising selecting the error correction code, signal constellation and the spreading code applied to a bitstream to provide a desired information transmission rate for the bitstream.

As per claim 75, Sakoda inherently includes, further comprising selecting the error correction code, signal constellation and spreading code applied to a bitstream based on signal transmission quality.

As per claim 76, Sakoda inherently includes further comprising selecting the error correction encoding rate, signal constellation and spreading code applied to a bitstream such that an information transmission rate for the bitstream is greater than a predetermined information

transmission rate and a signal transmission quality for the bitstream meets a predetermined criterion.

As per claim 77, Sakoda inherently includes, further comprising selecting respective combinations of error correction code, signal constellation and spreading code applied to the respective bit streams of the plurality of bit streams such that the information.

As per claim 78, Sakoda inherently includes, further comprising controlling respective power levels at which respective ones of the plurality of bit streams are transmitted.

As per claim 79, Sakoda inherently includes, further comprising selecting respective combinations of error correction code, signal constellation and spreading code applied to the respective bit streams of the plurality of bit streams such that the information transmission rate for a first bittern is maximized while maintaining a desired transmit power level for the plurality of bit streams.

As per claim 80, Sakoda inherently includes, wherein spreading respective ones of the symbol streams according to respective spreading codes comprises spreading respective ones of the symbol streams according to respective combinations of an orthogonal spreading code of a set of orthogonal spreading codes and a common scrambling code.

As per claim 81, Sakoda inherently includes, wherein the set of orthogonal spreading codes comprises a set of Walsh-Hadamard codes.

As per claim 82, Sakoda includes, wherein the set of orthogonal spreading codes comprises a set of Fourier codes (see 107).

As per claim 83, Sakoda inherently includes, wherein generating respective symbol streams from respective ones of the respective encoded bit streams according to respective signal

constellations of a plurality of signal constellations comprises producing respective symbols from a signal constellation from respective groups of bits of an encoded bitstream such that a first bit position of the successive groups of bits correlates to clusters of signal plane constellation points of the selected signal constellation and a second bit position of the successive groups correlates to relative positions within the clusters of constellations points.

As per claim 84, Sakoda inherently includes, further comprising: determining respective first and second desired power levels for respective first and second recipients of information in respective ones of the first and second bit positions; and controlling spacing of the clusters of constellation points in the signal plane based on the determined first and second desired power levels.

As per claim 85, Sakoda inherently includes, further comprising: determining respective first and second desired power levels for respective first and second recipients; and assigning respective ones of the first and second bit positions to respective ones of the first and second recipients based on the determined first and second desired power levels.

As per claim 86, Sakoda inherently includes: wherein spreading respective ones of the symbol streams according to respective spreading codes comprises orthogonal spreading an error -correction encoded bitstream according to an orthogonal spreading code of a set of orthogonal spreading codes; and wherein generating respective symbol streams from respective ones of the respective encoded bit streams according to respective signal constellations of a plurality of signal constellations comprises generating a symbol stream from the orthogonal spread error correction encoded bitstream according to a signal constellation that maps complementary bit patterns to diametrically opposite constellation points in a complex plane.

As per claim 87, Sakoda inherently includes, wherein spreading respective ones of the Symbol stream according to respective spreading codes comprises modulo 2 adding bits of the orthogonal spreading code to successive groups of bits of the error correction encoded bitstream.

As per claim 88, Sakoda inherently includes, wherein the plurality of error correction codes comprise at least one of a convolutional code, a Trellis code, a turbo code, and a serial concatenation of a first error correction code, interleaving and a second error correction code.

As per claim 89, Sakoda inherently includes, wherein the plurality of signal constellations comprises at least one of a QPSK constellation, an 8-PSK constellation, an M-ary PSK constellation, and a M-ary QAM constellation.

As per claim 91, Sakoda inherently includes, further comprising: determining respective first and second desired power levels for respective first and second recipients of information in respective ones of the first and second bit positions; and controlling spacing of the clusters of constellation points in the signal plane based on the determined first and second desired power levels.

As per claim 92, Sakoda inherently includes: determining respective first and second desired power levels for respective first and second recipients; and assigning respective ones of the first and second bit positions to respective ones of the first and second recipients based on the determined first and second desired power levels.

As per claim 93, Sakoda inherently includes: despreading first and second received signals according to respective first and second spreading codes; generating respective first and second symbol estimates from the respective first and second despread first and second received signals; decoding the first symbol estimate according to a combination of a first error correction

code and a first signal constellation; and decoding the second symbol estimate according to a second combination of a second error correction code and a second signal constellation.

As per claim 94, Sakoda inherently includes, wherein the first and second signal constellations are of different orders.

As per claim 95, Sakoda inherently includes, wherein the first and second error correction codes have different rates.

As per claim 96, Sakoda inherently includes, wherein the first and second spreading codes have different lengths.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 55-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Willming U.S. Patent No 5,923,711.

As per claims 55 62 and 65, Willming discloses a method of communicating a bitstream, comprising: modulo-2 adding (see fig.3 elements 54, 62 and col.5, lines 32-67) each bit of a binary spreading code of length N in turn to a first group of bits of the bitstream to generate a revised first group of bits; generating a first symbol from the revised first group of bits using a signal constellation that maps (see fig.3 element 22 and col.5, lines 60-67 and col.6, lines 13-35) the first group of bits and a complement of the first group of bits to diametrically opposite constellation points; and transmitting (see fig.1 element 10 and col.3, line 54) the first symbol in a communications medium.

As per claim 56, Willming inherently includes, wherein the bitstream includes a second group of bits, and further comprising: translating the second group of bits to the first group of bits; modulo-adding each bit of a binary spreading code of length N in turn to the translated second group of bits to generate a revised translated second group of bits; generating a second symbol from the revised translated second group of bits using the signal constellation that maps the first group of bits and a complement of the first group of bits to diametrically opposite constellation points; and transmitting the second symbol in the communications medium.

As per claim 57, Willminga inherently includes, wherein translating the second group of bits to the first group of bits comprises translating the second group of bits to the first group of bits by cross-reference to a look-up table.

As per claim 58, wilming inherently includes: wherein transmitting the first symbol in a communications medium is preceded by scrambling the first symbol according to a scrambling code; and wherein transmitting the first symbol in a communications medium comprises transmitting the scrambled first symbol in the communications medium.

As per claim 59, Willming inherently includes, wherein the scrambling code comprises a complex sequence.

As per claim 60, Willming inherently includes, wherein the complex sequence comprises binary-valued real and imaginary components.

As per claim 61, Willming inherently includes, wherein scrambling the first symbol according to a scrambling code comprises multiplying the first symbol by a scrambling sequence value.

As per claim 63, Willming inherently includes, wherein the signal constellation comprises a 16-QAM constellation in which the at least one sub-group of equally spaced constellation points comprises four subgroups angularly spaced at 90 degree intervals.

As per claim 64, Willming inherently includes, wherein the one-to-one mapping comprises a lookup table.

As per claim 66, Willming inherently includes, wherein the numbers of times each group of bits is used to form symbols for each of the group of recipients is the same.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Li et al U.S. Patent no 6,324,209 B1 teaches a multi channel spread spectrum.

Mui U.S. patent No 6,690,739 B1 teaches a method for intersymbol interference.

Wheatly, III et al U.S. Patent no 6,307,840 B1 teaches a mobile station assisted timing synchronization in CDMA.

Honda U.S. patent N0 6,498,789 B1 teaches a CDMA mobile.

Dejaco U.S. patent No 6,205,130 B1 teaches a method and apparatus for detecting bad data packets.

Asada et al U.S. patent No 6,553,535 B1 teaches a power efficient communication.

Wei U.S. patent No 6,421,395 B1 teaches a termination of coded.

Markman et al U.S. patent no 6,449,002 B1 teaches a truncated metric.

Rinchiuso et al U.S. Patent No 6,144,651 teaches a data transmission.

Citta et al U.S. patent No 5,636,251 teaches a receiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 703 308-9573. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 703 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

Wednesday, March 03, 2004